

### **Purpose and Importance**

### What Is Our Project About?

The project serves as a proof of concept for using a RISC-V processor on the mainboard of a laptop designed for deep-space missions. Leveraging NASA and Microchip's High-Performance Spaceflight Computing (HPSC) processor, this project demonstrates the feasibility of a resilient, energy-efficient laptop capable of withstanding space radiation.

### **Radiation Threats to Hardware**

- Single Event Effects (SEE) can disrupt electronic components when high-energy particles strike a device. These effects can cause bit shifts, altering the state of a circuit (e.g., changing a '0' to a '1'), which may lead to software errors or system crashes.
- Total lonizing Dose (TID): Causes undesirable charge collection at silicon and insulator interfaces, leading to performance issues and potential failure over time.TID can permanently damage components as the degradation accumulates.
- Displacement Damage Dose (DDD): Displaces atoms in silicon/dopant lattice structures, creating defects that impair device performance. DDD can also lead to permanent damage in affected components.

# **Design Objective**

- **Processor Selection:** The HPSC processor is currently being developed. We've decided to prototype using the MicroChip PolarFire. Like the HPSC, this processor is RISC-V and staying in the Microchip ecosystem allows for more seamless integration of the HPSC when it is released
- Project Goal: Design a schematic and PCB layout for a laptop mainboard compatible with a laptop chassis.
- Reference Design: We are using the PolarFire Icicle kit to test the functionality of the microprocessor. We have decided to use the Icicle Kit as a reference to aid in the design of our custom mainboard. We will customize the layout by:
- Removing non-essential components

Connectivity

Options

- -Integrating necessary features (video, audio, storage, display, network connectivity)
- Expected Outcome: A proof of concept RISC-V based mainboard suitable for future design toward a HPSC based radiation tolerant mainboard.



**Increased Radiation** 

Tolerance

# **RADIATION-TOLERANT CREW LAPTOP**

# Aidan Bachmeyer, Daniyar Boztayev, John Gellerup, Alex Johnston, Josh Muniga, Hunter Savage-Pierce Texas State University - Effectively Grounded

### Laptop Mainboard Implementation







Fig. 4: Doom Running on Icicle Kit Development Board Example

We used the Icicle Development board to create a minimum viable product demonstrating the functionality of the PolarFire SoC FPGA. We will take what we learned and apply it to our custom mainboard that we are designing. By testing the functionality of each component we will ensure they will work in a RISC-V ISA ecosystem. Our custom PCB will lay the foundation for a high-performance, radiationtolerant crew laptop.



Fig. 5: Icicle Kit Development Board (Courtesy of Microchip)



Fig. 6: HPSC Processor (Courtesy of Microchip)



- Booted Linux on Icicle Kit and Tested its Capabilities.
- Conducted trade study for available RISC-V processors.
- Established direct contact with Microchip to aid board design.



### **Next Steps and Development Goals:**

- board.



The Radiation-Tolerant Crew Laptop project provides a path toward a HPSC processor based crew laptop suitable for deep space missions. Our project will work as a proof of concept, so future teams can build off our design and work toward an HPSC based laptop.

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### Accomplishments

• Completed Most of the Schematic for our custom PCB board.

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VDDI VDD2				

Fig. 7: Examples of Completed Schematics

# Path Forward

• PCB Design Finalization: Complete the custom PCB layout and schematic to incorporate all necessary components for space operation. • Prototype Fabrication and Assembly: Once the design is finalized, proceed with fabricating and assembling an initial prototype of the main-

• System Integration Testing: Perform comprehensive tests to ensure the successful integration of core components, such as the RISC-V processor, memory, and peripheral interfaces (video, audio, and network).

• Firmware and Software Optimization: Work on firmware modifications and software layers to optimize the functions of the laptop.

### A Platform for Continuous Innovation:

# Acknowledgements