Radiation-Tolerant Crew Laptop

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Purpose and Importance

What Is Our Project About?

The project serves as a validation suite for the mainboard being designed using a RISC-V processor laptop designed for deep-space missions. Leveraging NASA and Microchip's High-Performance Spaceflight Computing (HPSC) processor, this project demonstrates the feasibility of a resilient, energy-efficient laptop capable of withstanding space radiation.

Radiation Threats to Hardware

- **Single Event Effects (SEE)** can disrupt electronic components when high-energy particles strike a device. These effects can cause bit shifts, altering the state of a circuit (e.g., changing a '0' to a '1'), which may lead to software errors or system crashes.
- **Total Ionizing Dose (TID)**: Causes undesirable charge collection at silicon and insulator interfaces, leading to performance issues and potential failure over time.TID can permanently damage components as the degradation accumulates.
- **Displacement Damage Dose (DDD)**: Displaces atoms in silicon/dopant lattice structures, creating defects that impair device performance. DDD can also lead to permanent damage in affected components.

Design Objective

- **Project Goal:** Create a validation suite for the Polarfire Icicle Kit that can be translated to the Biz Board when the board is ready for testing.
- **Reference Design:** We are using Baremetal examples to test the functionality of all components that need to be tested. We have decided to use the Icicle Kit as a reference due to its similarity to the redesigned Biz Board. Some of these baremetal examples include.
  - DDR baremetal example
  - UART baremetal example
  - SPI slave master baremetal example
  - USB HID baremetal example
- **Expected Outcome:** A validation suite suitable for future design toward a HPSC based radiation tolerant mainboard.

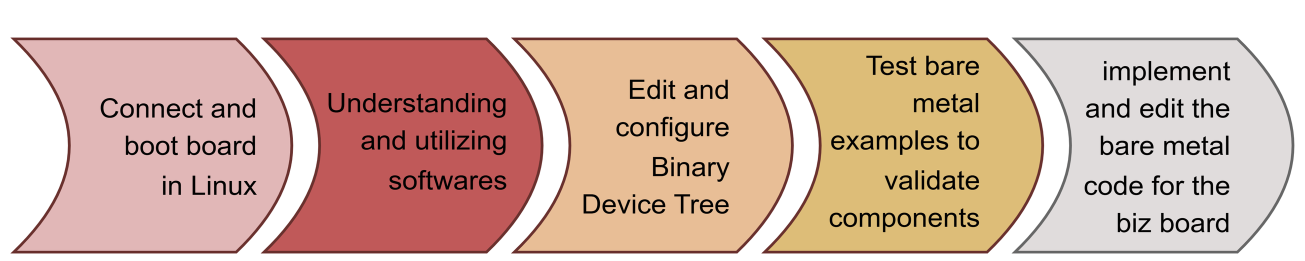

Fig. 1: Design Objectives

Board Features

Fig. 2: Subsystems

Laptop Mainboard Implementation

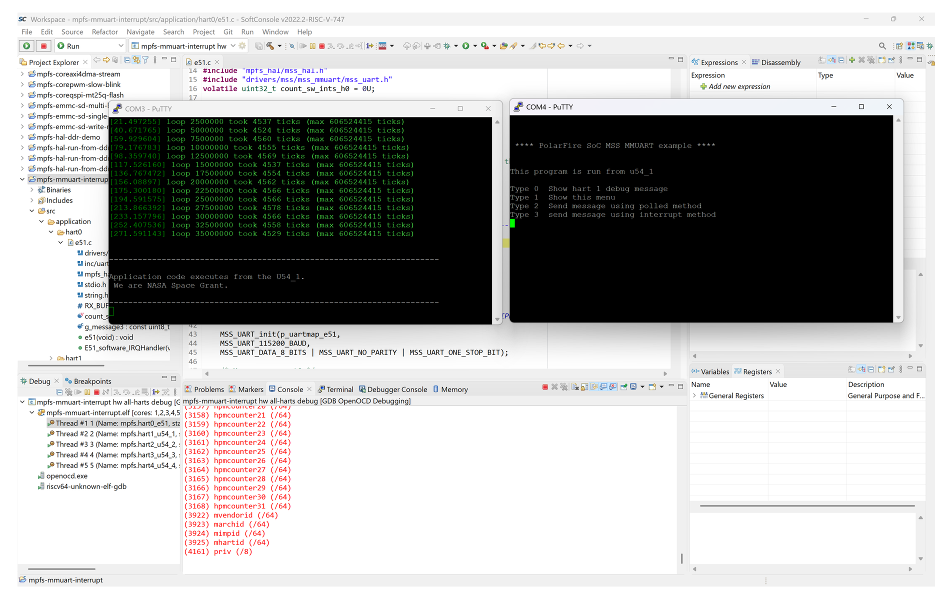

Fig. 3: Example of Baremetal Code

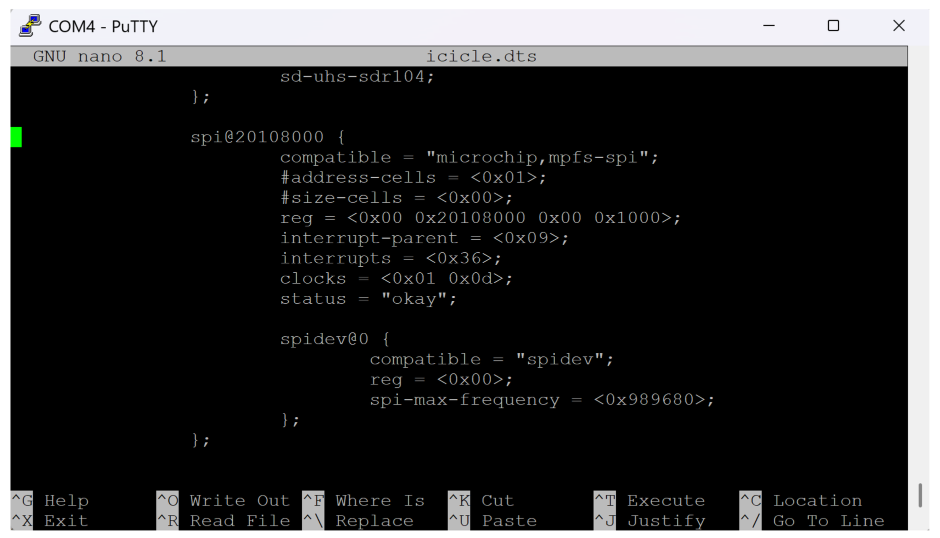

Fig. 4: Device Tree Example

We used the Icicle Development board to create a validation suite demonstrating functionality of all components that will need testing on the redesigned Biz Board. By testing the functionality of each component we will ensure they will work in a RISC-V ISA ecosystem. Our validation suite serve as a foundation for all code associated with testing and debugging for the final radiation-tolerant crew laptop.

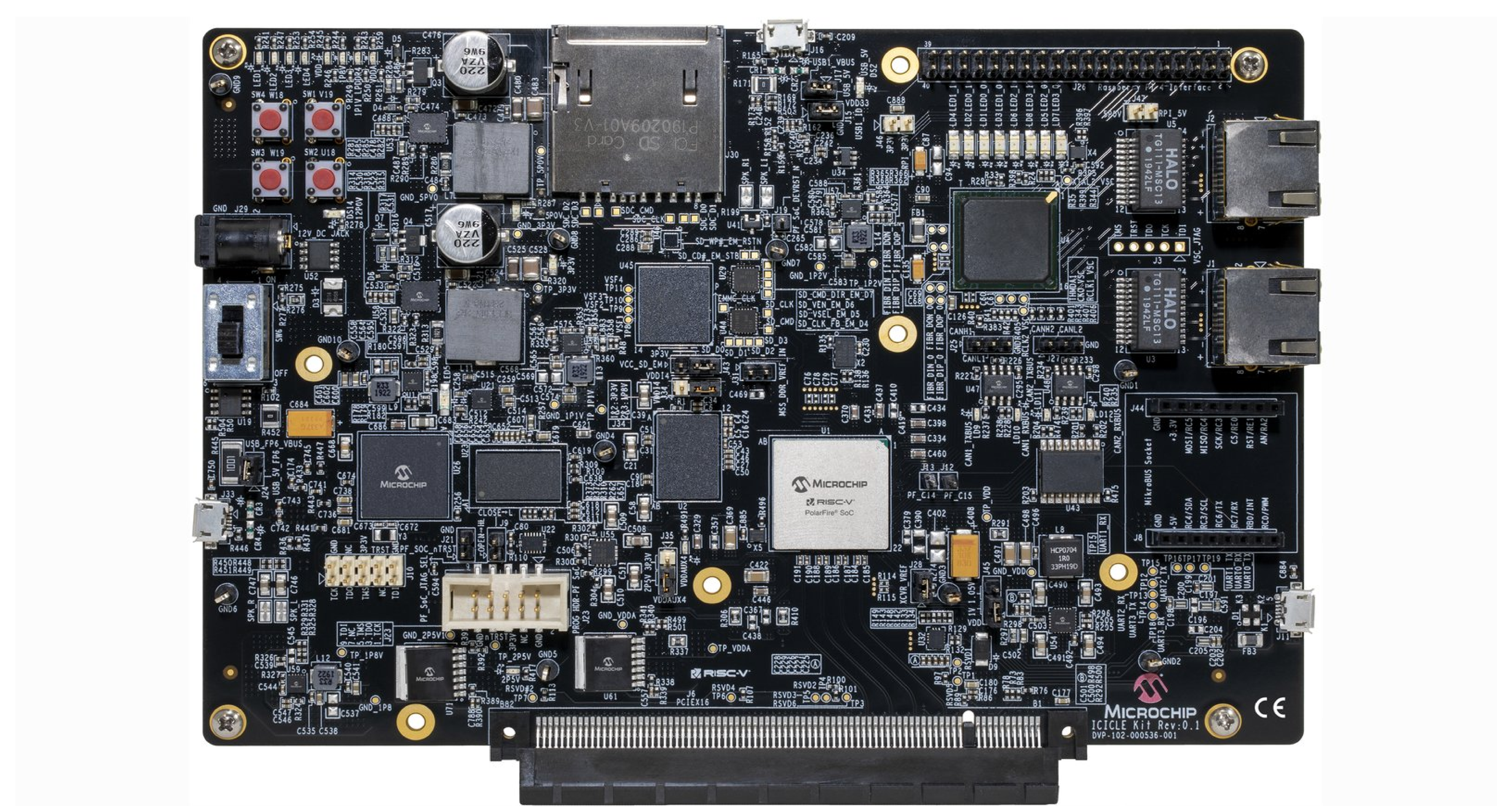

Fig. 5: Icicle Kit Development Board (Courtesy of Microchip)

Fig. 6: HPSC Processor (Courtesy of Microchip)

Accomplishments

- Successfully booted Linux on Icicle kit allowing us to navigate through and edit the device tree and file system of the board.
- Successfully used SoftConsole to edit and run all code associated with the Icicle Kit.
- Found and edited baremetal code examples to validate the components of each subsection.
- Found and edited the HSS boot loader code for the Icicle kit allowing for a more detailed boot helping detect any errors during the boot process.
- Successfully found a method of switching between boot modes allowing the board to boot as expected for each modes use.

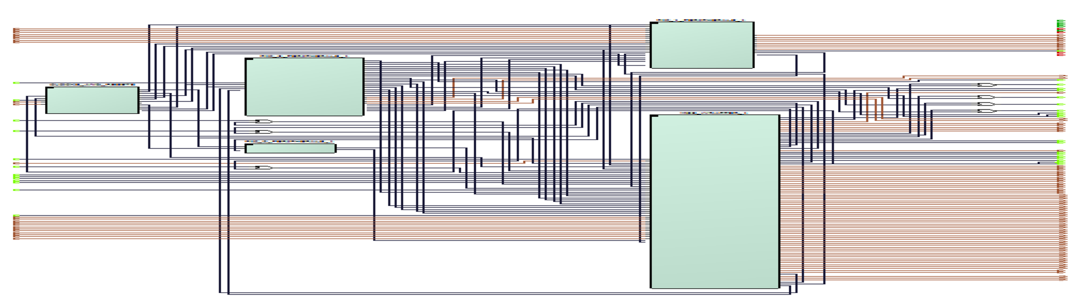

Fig. 7: Libero FPGA Design

Path Forward

Next Steps and Development Goals:

- Verify functionality of all baremetal examples and ensure that they allow for full validation of each component needed to be tested.
- Integrate all baremetal examples needed for the Biz Board in order to accommodate for any changes made from Icicle to Biz Board
- Optimizing firmware and software to improve functionality and efficiency

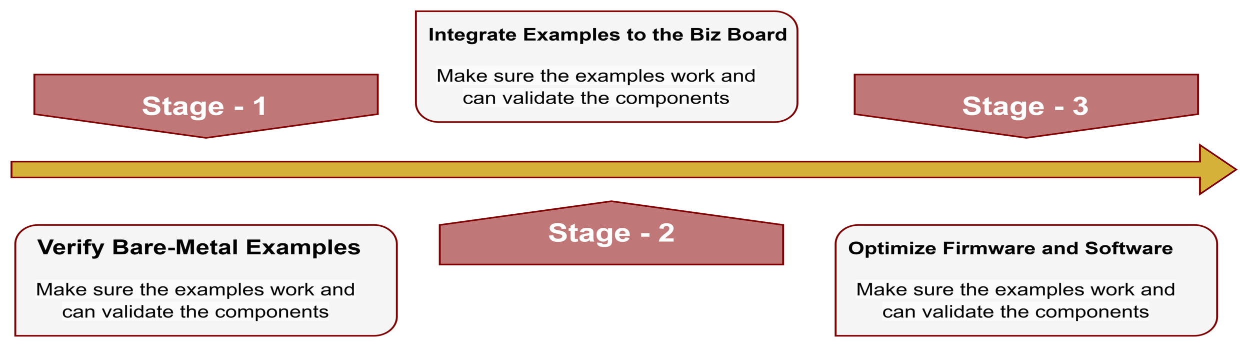

Fig. 8: Future Goals

A Platform for Continuous Innovation:

The Radiation-Tolerant Crew Laptop project provides a path toward a HPSC processor based crew laptop suitable for deep space missions. Our project will work as a proof of concept, so future teams can build off our design and work toward an HPSC based laptop.

Acknowledgements

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