TDC-103 Radiation-Tolerant Crew Laptop

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Texas State University - Effectively Grounded

Purpose

The project serves as a proof of concept for using a RISC-V processor on the mainboard of a laptop designed for deep-space missions, leveraging Microchip's High-Performance Spaceflight Computing (HPSC) processor.

Radiation Threats to Hardware

- **Single Event Effects (SEE)** can disrupt electronic components when high-energy particles strike a device, which may lead to software errors or system crashes.
- **Total Ionizing Dose (TID)**: Causes undesirable charge collection at silicon and insulator interfaces, leading to performance issues and potential failure over time.

Scope

Since the HPSC processor is still under development, our team opted to use Microchip's PolarFire SoC FPGA. The primary objective of the project's first phase was to demonstrate the feasibility of a RISC-V-based mainboard for a laptop and to complete the schematic design. The second phase focuses on finalizing the initial board layout and preparing it for manufacturing.

Mainboard v1.0 Form Factor

Future projects will adapt the design for compatibility with the HPSC processor and the Framework 16 mainboard through an iterative process aimed at developing a radiation-tolerant crew laptop.

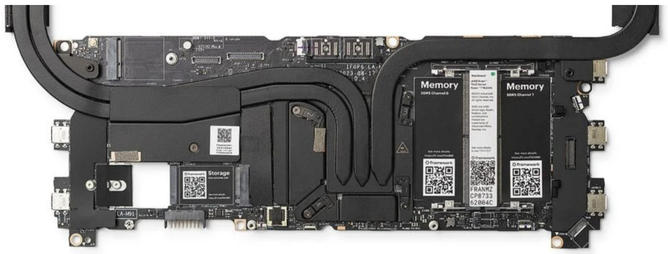


Figure 1: Framework 16 Mainboard

Subsystems

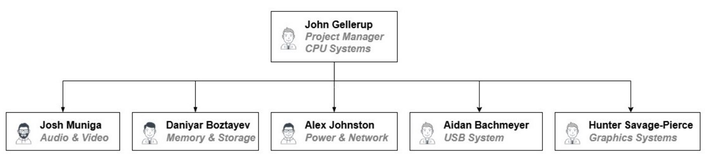


Figure 2: Left to Right: Alex Johnston, Hunter Savage-Pierce, Daniyar Boztayev, Josh Muniga, John Gellerup, Aidan Bachmeyer

Laptop Mainboard Implementation

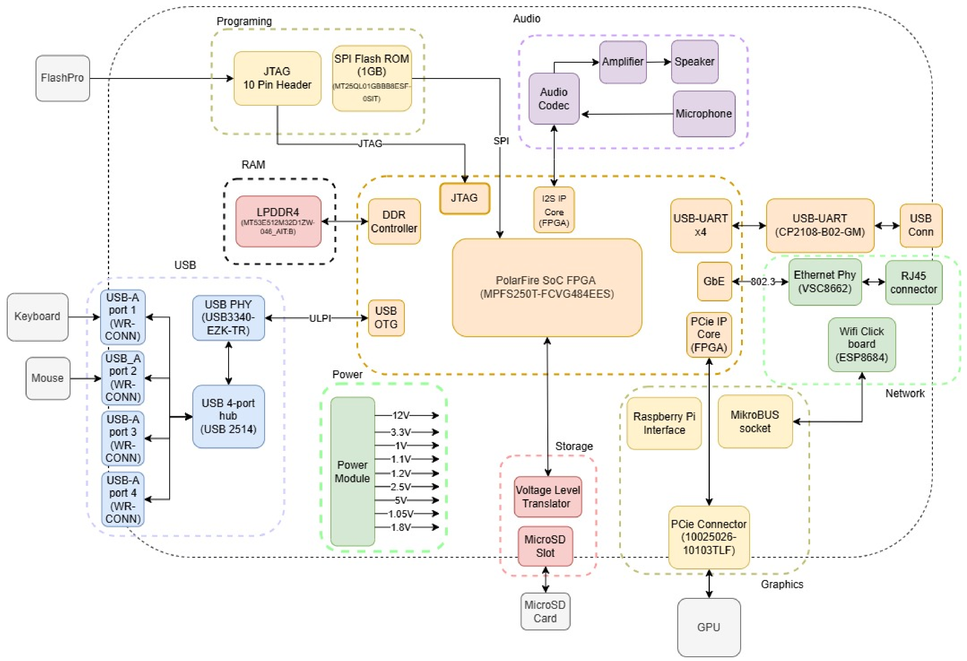


Figure 3: Top-level block diagram of the laptop mainboard.

Accomplishments

Schematic Capture

- **Review:** Conducted comprehensive schematic reviews to verify critical circuit connections, ensure functionality, and confirm integration across all schematic sheets.
- **Design:** Developed clear, well-structured multi-page schematics to guide an effective board layout phase.
- **Standards:** Integrated industry-standard design practices resulting in error-free schematics.

PCB Layout

- **Fanout:** Successfully completed the fanout of the PolarFire SoC Ball Grid Array (BGA), using vias to access internal layers and manage dense signal routing.
- **New Additions:** Introduced USB-hub and video capabilities, along with an audio system interfaced through the Field-Programmable Gate Array (FPGA).
- **Progress:** Populated the majority of the board with components and began routing critical signals.

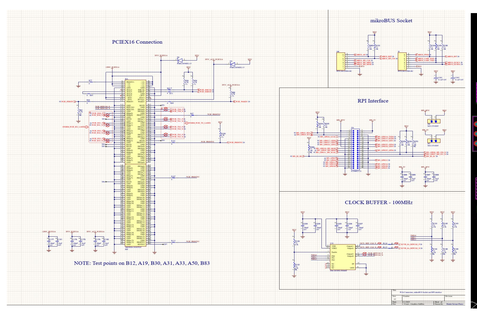


Figure 4: Altium Schematic of PCIe Interface.

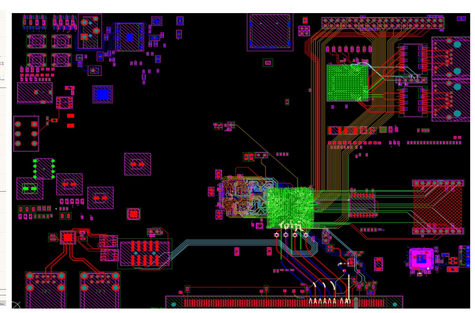


Figure 5: Altium Layout Design of the Board

Future Development

Development Road Map:

- Finalize PCB layout, including trace routing, layer stack adjustments, and design rule checks.
- Manufacture board through external fabrication service.
- Conduct verification and validation through design checks, probing key nets, and performing bring-up tests to ensure proper system behavior.
- Modify existing design to support integration with the HPSC.
- Refactor board layout to achieve the target form factor.

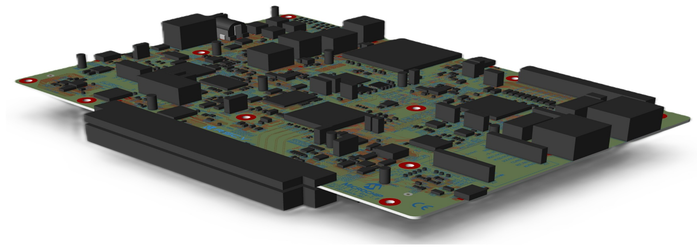
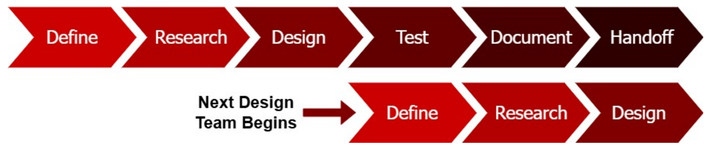


Figure 6: Icicle Kit 3D model (Courtesy of Microchip)

Project Flow

Each design team works on the project for two full semesters. Incoming teams join after the first semester and collaborate with the current team during their final semester to ensure a smooth transition.



A Platform for Continuous Innovation:

Our team has designed the USB-hub and audio solutions, which brings the design of the mainboard closer to the final product. By adding these features, we will get closer to the functionality of the desired product. The future teams will add more features and build off of our design that will eventually reach the goal of this project.

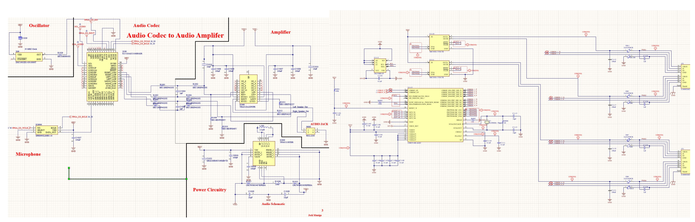


Figure 6: Audio and USB Schematics

Acknowledgments

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