Radiation-Tolerant Crew Laptop

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Purpose and Importance

What Is Our Project About?

NASA is seeking a powerful, energy-efficient laptop capable of operating in the extreme conditions of cis-lunar travel for the upcoming Artemis missions. In this environment, digital electronics are exposed to ionizing radiation, which can permanently damage mission-critical components such as the processor. To address these challenges, the High-Performance Spaceflight Computing (HPSC) RISC-V processor, developed by Microchip, is being introduced as a radiation-tolerant solution. Our role is to design a crew laptop built around the HPSC processor while maintaining the form factor of the Framework 16 laptop.

Design Objective

- **Project Goal:** Define the high-level architecture for a radiation-tolerant crew laptop using the Framework 16 platform as a reference. This architecture definition encompasses the communication protocols, interfaces, and subsystem devices integrated into the overall design.
- **Challenges:** The HPSC processor has limited built-in communication interfaces, which creates challenges because the Framework ecosystem depends on a wide range of I/O interfaces to operate correctly.

Design Features

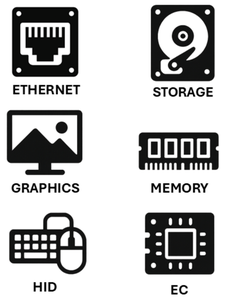

Fig. 1: Subsystems

Acknowledgements

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High-Level Architecture Design

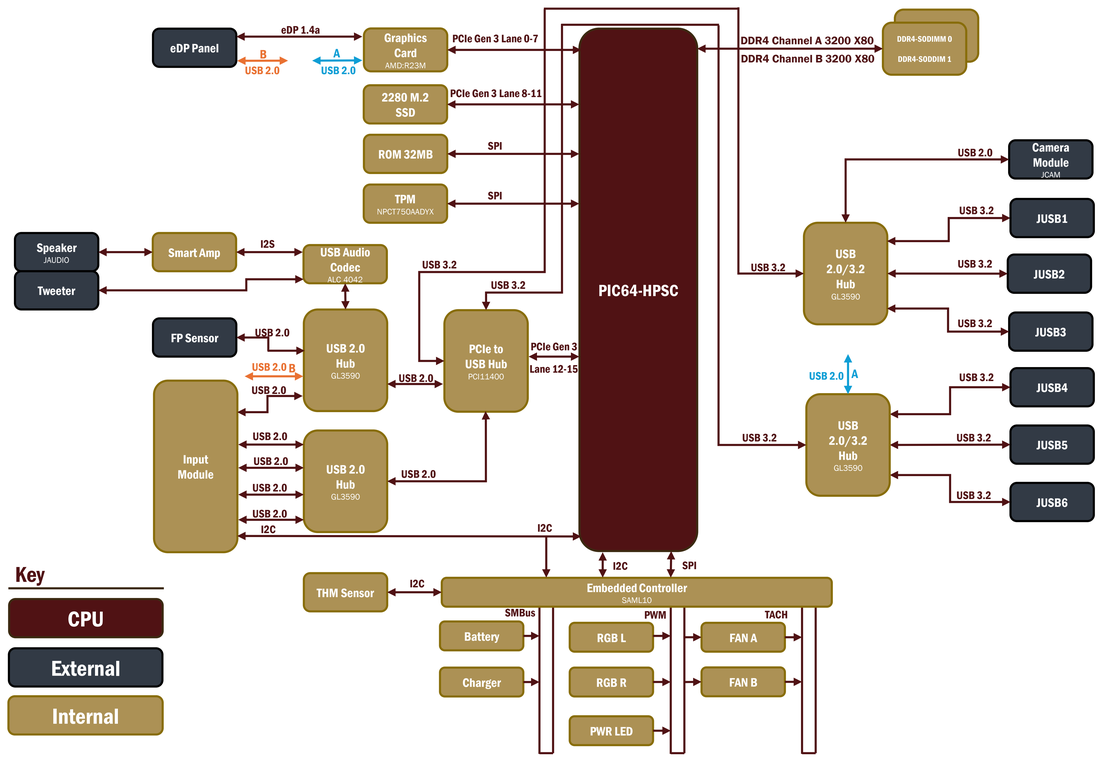

Fig. 2: High-Level Diagram

Future Development

A Platform for Continuous Innovation:

The Radiation-Tolerant Crew Laptop project provides a path toward a HPSC processor based crew laptop suitable for deep space missions. Our project will serve as a proof of concept, allowing future teams to build off our design and work toward an HPSC based laptop.

Next Steps

Future teams will be responsible for continuing the development of the HPSC-based Framework laptop. They will use the high-level architecture we defined to create a full schematic and fabricate the PCB. Once the hardware is built, the validation tools we developed will be used to verify the functionality of each subsystem and confirm the design meets project requirements.

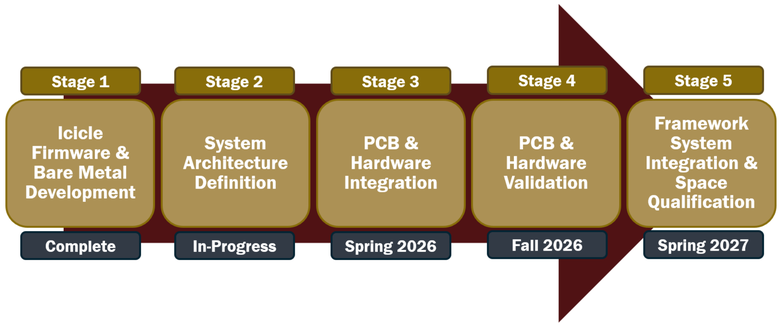

Fig. 3: Path Forward

Radiation Threats to Hardware

- **Single Event Effects (SEE):**
  High-energy particles can flip bits or disrupt circuits, leading to software errors or system crashes.
- **Total Ionizing Dose (TID):**
  Long-term radiation buildup degrades device performance and can permanently damage components.
- **Displacement Damage Dose (DDD):**
  Radiation displaces atoms in the silicon lattice, creating defects that reduce reliability and may cause permanent failure.

Accomplishments

Spring 2025 Semester

- **Modified HSS Bootloader:**
  Customized the HSS bootloader for our system's startup sequence and mapped each boot stage to the planned subsystem bring-up order. We then verified the boot process through multi-stage logging and confirmed the expected UART output.
- **PolarFire SoC Research:**
  Researched the PolarFire SoC ecosystem and SoftConsole workflow, creating documentation and early development tools to support future debugging and bring-up of the HPSC-based mainboard.
- **Bare-metal Example Testing:**
  We modified and deployed bare-metal firmware on the PolarFire Icicle Kit, using SoftConsole to compile, debug, and flash multi-hart RISC-V applications while validating hardware communication for the HPSC prototype.

Fall 2025 Semester

- **High-Level Architecture Defined:**
  Developed the high-level system architecture for a radiation-tolerant crew laptop using the Framework 16 chassis and HPSC (RISC-V) processor, incorporating PCIe, USB, DDR4, and peripheral subsystems.
- **Solved the USB Interface Gap:**
  Identified a critical architectural limitation and engineered a working solution using the PCI11400 PCIe-to-USB host controller and the GL3590 multi-port USB 2.0/3.2 hub.
- **Collaboration with Mentee Group:**
  Partnered with RadDawgs to explore device alternatives, align requirements, and share technical insights (e.g., on the PCI11400).