

# Radiation-Tolerant Crew Laptop USB Hub Development Board - Project Overview

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NASA Sponsor: Justin R. Bautista Faculty Advisor: Jeff Stevens

## Background

The space radiation environment is severely disruptive to conventional electronics, limiting the compute capability available for space-based systems. Software errors or system crashes may occur due to **Single Event Effects (SEE)** wherein high-energy particles flip bits or disrupt circuits. Semiconductor lattices are degraded overtime through a process called **Displacement Damage (DD)** wherein heavy or extremely high energy particles impact and displace the individual atoms within a crystal lattice. To analogize, picture charges traveling through a semiconductor as cars traveling down a highway; displacing atoms is like cratering that roadway. Furthermore, insulators within transistors are degraded over time through a process called **Ionization** wherein high energy particles (mainly photons) displace electrons from atoms, leaving a 'hole'. These 'holes' migrate to material interfaces over time where their presence facilitates **trap-assisted tunneling**, creates **parasitic channels**, and causes **subthreshold swing degradation**.

These problems led NASA to begin designing the Radiation-Tolerant Crew Laptop. Microchip's radiation-tolerant PIC64-HPSC will serve as the CPU for a modular system based on the Framework 16 Laptop. Previous Texas State University Senior Design Teams developed a high-level preliminary system design and created a PCIe to USB Host Controller so the HPSC could serve as the CPU for a Framework 16 style system. Team Redtops' mission is to create a USB Hub Development Board to test a viable architecture that meets the Framework 16 based system requirements.

## Design Solution

As can be seen in the **USB Hub** and **Laptop Top Level Block Diagrams**, our USB Hub Development Board routes data between **eight downstream ports** and **two upstream ports**. The downstream ports consist of three **Type-C USB 3.2 Gen 2** ports and five **Type-A USB 2.0** ports, while the upstream side contains one USB 3.2 Gen 2 port and one USB 2.0 port. To achieve full data connectivity, the final motherboard would need to instantiate a left and right version of this architecture.

Since the Framework 16 Laptop receives system power through its USB subsystem, we too have incorporated a method to receive system power through the USB subsystem. We are designing our board to be capable of sinking 240W, just like the Framework 16 advertises, through a single **USB PD3.1 EPR** capable USB port. We are also building in the ability to source 5V, 20V, or 48V through that same port for temporarily providing power to external devices. Referring to our **USB Hub Power Subsystem Block Diagram** will also show that we are integrating **Dead Battery Support**, so a Crew Laptop with a completely drained or malfunctioning battery will still be able to turn on and operate when external power is connected.

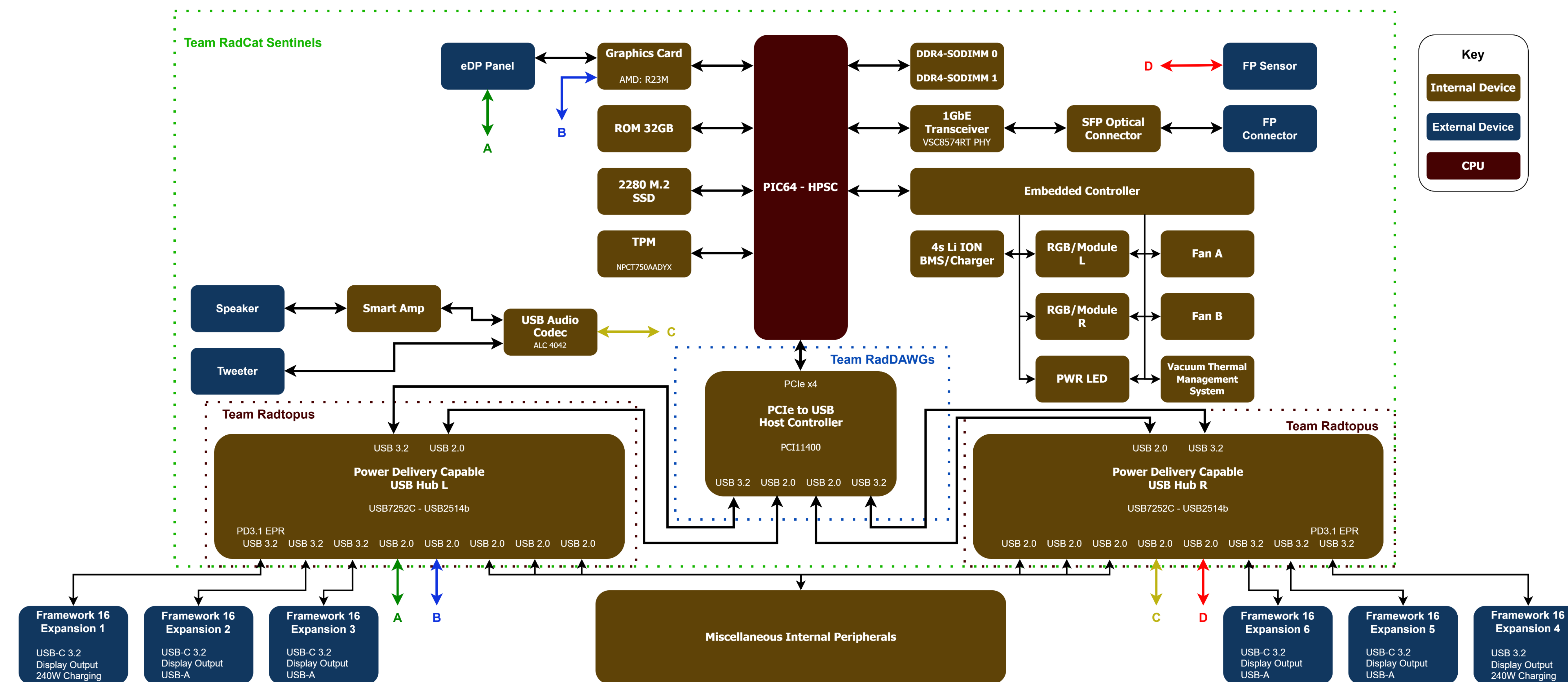
## Design Philosophy

Our team's design philosophy is to create a dev board that will serve as a strong reference design for the final rad-tolerant crew-laptop USB subsystem, emphasizing radiation robustness, thermal resilience, and architectural clarity from the outset. As such, we:

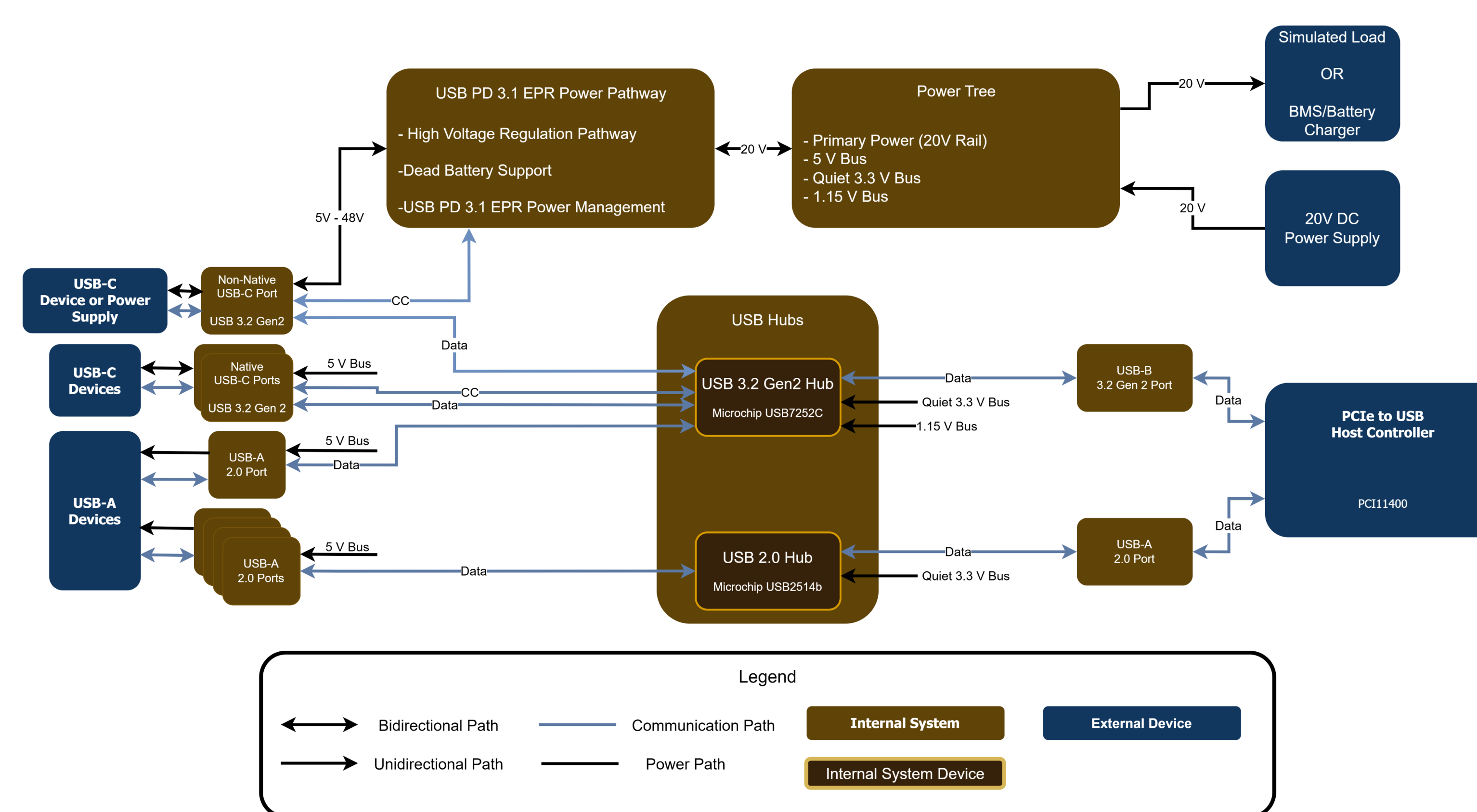
- favor **analog control over digital configurability** to reduce SEE susceptibility
- treat thermal performance as a mission-critical** constraint given the challenges of heat rejection in space and lunar environments
- place strong **emphasis on high-fidelity signal integrity** to ensure reliable high-speed communication in a radiation-affected environment
- maintain an eye towards follow on development** by building in power connections for a follow-on 4s Li-ion Battery Management System/Charger, and cataloging every component's radiation posture to not only identify available rad-tolerant alternatives but also to highlight where NASA may need future rad-tolerant device development

The result will be a commercial off-the-shelf-based prototype with a clear, well-documented path towards creating a fully rad-tolerant, space-ready device.

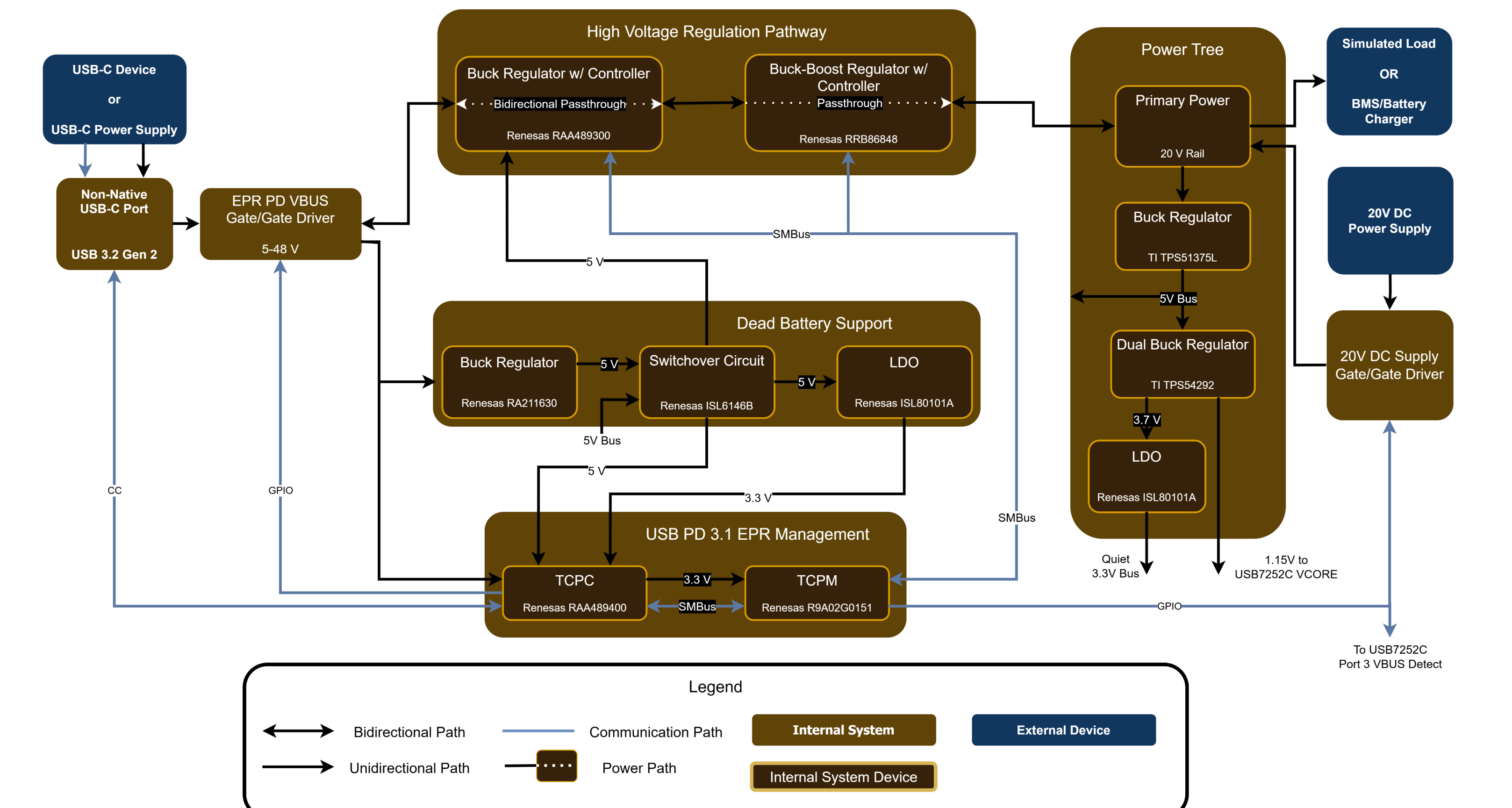
## Laptop Top Level Block Diagram



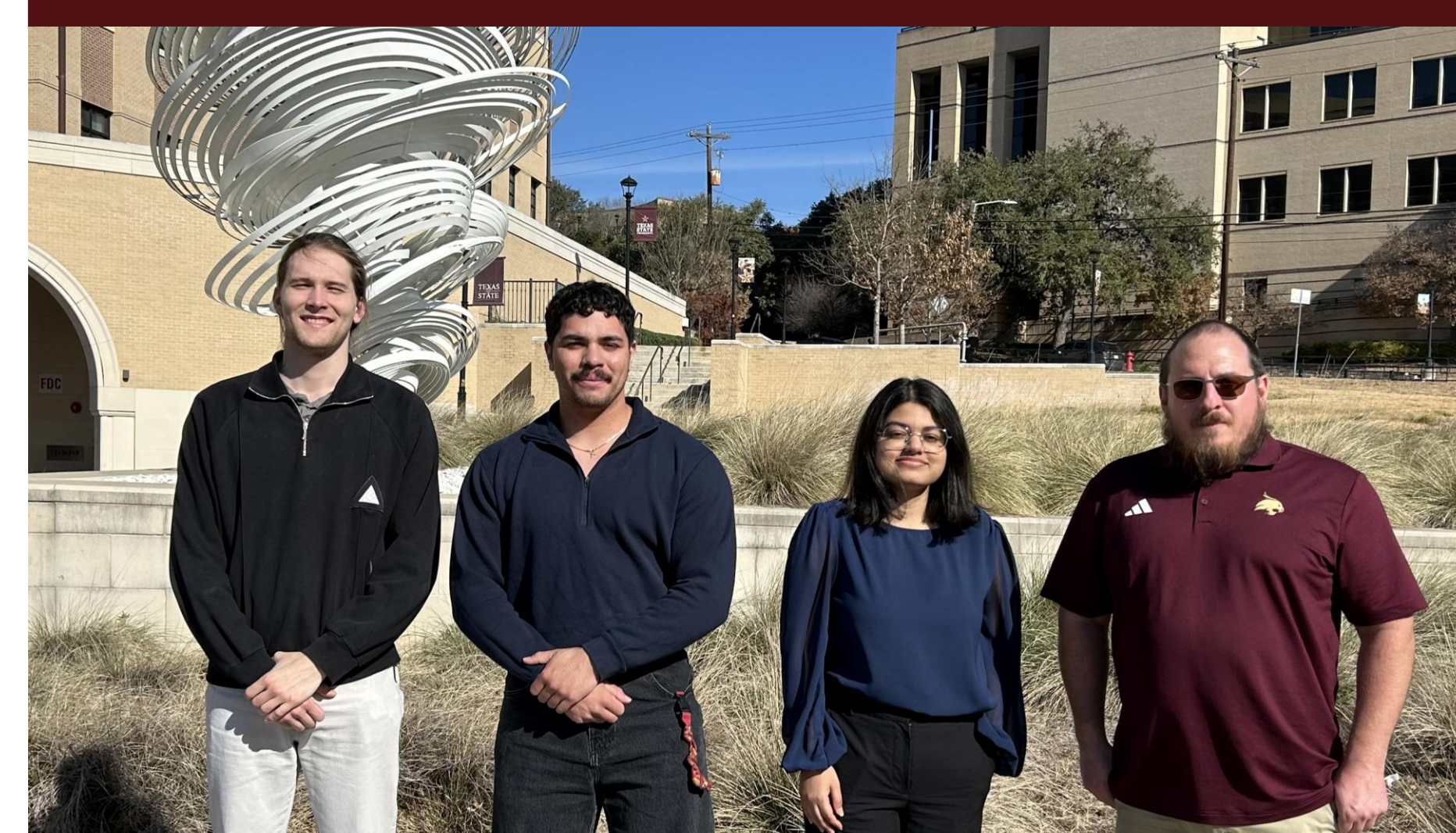
## USB Hub Top Level Block Diagram



## USB Hub Power Subsystem Block Diagram



## Team



From left to right:  
 Matthew Giddens  
Lead: High Speed Routing, PCB Layout  
 Javier Garcia  
Lead: Power Delivery and Protection  
 Rabea Fatima  
Lead: Hub Configuration, Validation, Testing  
 Cameron Guillies – PM  
Lead: System Integration, DFM, DFT

## Acknowledgements

We extend our gratitude to our NASA sponsor, Mr. Justin Bautista, our Texas State University Faculty at large, and Mr. Mark Welker and Mr. Jeffery Stevens in particular, for making opportunities like this possible. We would also like to sincerely thank the afore mentioned individuals for their guidance and support while working on this project. Additionally, we would like to acknowledge the educators in our life that have assisted in our academic growth. Finally, we would like to make known our appreciation for those technical writers and product engineers who compose clear and informative data sheets.

Questions, comments and concerns regarding our project may be directed to Cameron Guillies

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## Project Schedule

Phase	Task	Timeline
Phase 1	Design Philosophy and Development Board Architecture Definition	Spring 2026
Phase 2	Development Board Schematic Creation	Spring 2026
Phase 3	PCB Layout	Fall 2026
Phase 4	Fabrication Prep and Release	Fall 2026
Phase 5	Development Board Validation and Testing	Fall 2026
Phase 6	Final Documentation Generation and Release	Fall 2026

## Accomplishments

**Development Board Architecture Defined:** 8 down, 2 up USB hub with Extended Power Range Power sinking/sourcing, downstream battery charging support, and power terminal connections for a test load or follow-on 4s Li ion battery charging through our board.

**Design Philosophy Defined:** Refer to Design Philosophy section at lower left

**Schematic Creation:** Currently ~80% complete with the first draft of our schematics. On track for first draft schematic completion by 20 APR.